

## Designing Antenna Systems for Low Common Mode Current in Coaxial Feed

### Lines

Jacek Pawlowski, SP3L

The figures below show how two parallel RLC circuits connected in series placed in the same (last) segment #51 of wire #3 as you be input in the EZNEC (top) and 4nec2 (bottom) antenna editors.

Loads (RLC)											
Loads											
No.	Specified Pos.		Actual Pos.			R	L	C	R Freq	Config	Ext Conn
	Wire #	% From E1	% From E1	Seg	(ohms)	(uH)	(pF)	(MHz)			
1	3	100	99.0196	51	4400	620	6.7	0	Par	Ser	
2	3	100	99.0196	51	2750	59	6.7	0	Par	Ser	
*											

Edit NEC input-file										
Parallel RLC										
Card	Type	tag-nr	first-S	Last-S	Res (ohm)	Ind (H)	Cap (F)			
LD	1	3	51	51	2750	5.9e-5	6.7e-12			
CM Created from AutoEZ, converted with 4nec2 on 21-Oct-20 12:17 CE GW 1 53 0 0 19.1 0 -19.64 19.1 1.e-3 GW 2 53 0 0 19.1 0 19.64 19.1 1.e-3 GW 3 51 0 0 0 0 0 19.1 1.e-3 GE 1 LD 5 1 0 0 5.74713e7 0 LD 5 2 0 0 5.74713e7 0 LD 5 3 0 0 5.74713e7 0 LD 1 3 51 51 4400 0.00062 6.7e-12 LD 1 3 51 51 2750 5.9e-5 6.7e-12 EX 0 1 1 0 7.07107e-1 0 GN 3 0 0 0 13 0.005 FR 0 1 0 0 4 0										